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10/665,639	09/18/2003	Hiroki Koga	N34771600WD1	6100

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,639	KOGA, HIROKI	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7 and 17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-7 and 17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. With respect to claim 19, in fig. 8(a), as required in claim 17, the first IGFET includes a lightly doped drain and the second IGFET does not include a lightly doped drain. As in fig. 8a-d of the instant application, the region SA is a memory that does not include a lightly doped drain, while region SB is a peripheral that including a lightly doped drain 114B; thus the recited 'the first region is a memory cell region and the second region is a peripheral circuit region' is indefinite.

For the purpose of examination, the Examiner assumes the first region is a peripheral region and the second region is a memory region.

b. With respect to claim 20, for the reason stated above in claim 19, recited 'first gate electrode is <u>less</u> than a second spacing from second spacing from the second contact to the second gate electrode' is indefinite.

For the purpose of examination, the Examiner assumes 'first gate electrode is larger than a second spacing from second spacing from the second contact to the second gate electrode'.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 17 is rejected under 35 U.S.C. 102(b) as being anticipated by US 6030876 to Koike.

Regarding claim 17, Koike discloses a semiconductor device including a first region and a second region (left and right) in fig. 6C comprising: a first gate electrode of a first IGFET in the first region (right) having a first lower layer electrode 103 formed on a first gate insulating film 102 and a first upper layer electrode 121 formed on the first lower layer electrode 103; a first cap film 123 formed on the first upper layer electrode 121; a first nitride film 120 on a side surface of the first upper layer electrode 121; a first oxide film 103 on a side surface of the first lower layer electrode 103; a first etch stop film including a second nitride film 111 formed on the outside of the first nitride film 120 and first oxide film 106; a second gate electrode of a first IGFET in the first region (left side) having a second lower layer electrode 103 formed on a second gate insulating film 102 and a second upper layer electrode 121 formed on the second lower layer

electrode 103; a second cap film 123 formed on the second upper layer electrode 121; a third nitride film 120 on a side surface of the second upper layer electrode 121; a second oxide film 106 on a side surface of the second lower layer electrode 103; a second etch stop film including a second nitride film 111 formed on the outside of the second nitride film 120 and second oxide film 106; wherein the first IGFET includes a lightly doped drain 110, col. 8 line 23, and the second IGFET does not include a lightly doped drain, fig. 6C.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2-3, 5-7, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6030876 to Koike.

Regarding claim 1, Koike discloses a semiconductor device in fig. 6C including an insulated gate field effect transistor (IGFET), comprising: a gate electrode of the IGFET having a lower layer electrode 103, col. 5 line 60, formed on a gate insulating film 102, col. 5 line 58, and an upper layer electrode 121, col. 7 line 20, formed on the lower layer electrode 103; a cap film 123, col. 7 line 31, formed on the upper layer electrode 121, a first nitride film 120, col. 7 line 20, on a side surface of the upper layer electrode121; an oxide film 106, col. 6 line 3, on a side surface of the lower layer

electrode 103; and an etching stopper film including a second nitride film 111, col. 6 line 22, formed on the outside of the first nitride film 120 and an outside of the oxide film 106, wherein the first nitride film 120 does not cover the side surface of the cap film 123, fig. 6C. [0020].

But Koike does not disclose the first nitride has a film thickness of about 2 to 5 nm.

However, Koike discloses layer 120 has general thickness. Accordingly, it would have been obvious to one of ordinary skill in art to the thickness teaching of Koike in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 2-3, 6-7, the process limitations "thermal nitride film" in claims 2 and 6, "rapidly heated thermal nitride" in claim 3, and 'second nitride film id formed with CVD' of claim 7 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 5, Koike discloses the semiconductor device further including an interlayer insulating film 118 formed to cover the gate electrode of the IGFET; a contact hole 124, col. 7 line 59, opened in the interlayer insulating film 118 to expose a source/drain region 108, col. 8 line1, of the IGFET; and a conductor 125, col. 7 line 60, filling the contact hole and electrically connected the source/drain (S/D) region, fig. 6C.

Regarding claims 18-19, Koike discloses the semiconductor device is a semiconductor memory device, abstract, wherein the first region (right) is a peripheral circuit region, col. 6 line 6, and the second region (left) is a memory region, col. 6 line 11.

But Koike does not disclose the first and second nitride films have a thickness of about 6 nm.

However, Koike discloses layer 120 has general thickness. Accordingly, it would have been obvious to one of ordinary skill in art to the thickness teaching of Koike in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6030876 to Koike in view of US 6483138 to Habu et al.

Regarding claim 20, Koike discloses the semiconductor device further including: a second contact 125 providing an electrical connection to a second S/D of the second IGFET, fig. 6C.

But Koike does not discloses a first contact providing an electrical connection to a first S/D region of the first IGFET, and a first spacing from the first contact to the first gate electrode is greater than a second spacing from the second contact to the second gate electrode.

However, Habu discloses in fig. 19G wherein a first contact (right) providing an electrical connection to a first S/D region 8 of the first IGFET, and a first spacing from the first contact to the first gate electrode 2 is greater than a second spacing from the second contact (left) to the second gate electrode. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the contacts teaching of Habu with Koike's device, because it would have created a semiconductor device having a fine transistor capable of reducing resistance of the contact between a wiring layer and a diffusion layer and exhibiting excellent controllability by providing a large are for a contact hole formed in a self-align manner with a gate electrode as taught by Habu in col. 2 lines 58-65.

8. Claims 1-3, 5-7, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0132403 to Hung et al in view of US Pub 2002/0001935 to Kim et al.

Regarding claim 1, Hung discloses a semiconductor device in fig. 5 including an insulated gate field effect transistor (IGFET), comprising: a gate electrode of the IGFET having a lower layer electrode 6 [0018] formed on a gate insulating film 4 [0018], and an upper layer electrode 6a [0018], formed on the lower layer electrode 6; a cap film 8 [0019], formed on the upper layer electrode 6a, a first nitride film 12 [0002] on a side surface of the upper layer electrode 6a; an oxide film 10 [0018] on a side surface of the lower layer electrode 6; and an etching stopper film including a second nitride film 20

[0021] formed on the outside of the first nitride film 12 and an outside of the oxide film 10, wherein the first nitride film has a film thickness of about 5 nm [0020].

But Hung does not disclose the first nitride film does not cover the side surface of the cap film.

However, Kim discloses a semiconductor device in fig. 2H including a lower gate electrode 22a disposed on a gate-insulating layer 21, and an upper gate electrode 29 disposed on the lower gate electrode 22a, an oxide film 24 on the side surface of the lower electrode 22a and a nitride film 25 on a side surface of the upper gate electrode 29, fig. 2H. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the nitride film 25 teaching of Kim with Hung's device, because it would have prevented transformation of the gate electrode as taught by Kim, see abstract.

Regarding claims 2-3, and 6-7, the process limitations "thermal nitride film" in claim 2, "rapidly heated thermal nitride' in claim 3, "thermal oxide film' in claims 6, 23, and "nitride film is formed with CVD' in claims 7, 24 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 5, Hung discloses the semiconductor device further including an interlayer insulating film 22 [0022] formed to cover the gate electrode of the IGFET; a contact hole 24, fig. 3c, opened in the interlayer insulating film 22 to expose a source/drain region 15, fig. 3c, of the IGFET; and the source/drain region 16.

But Hung does not disclose the filling the contact hole and electrically connected the S/D region. At the time the invention was made; it would have

been obvious to one of ordinary skill in the art to understand that the contact hole 24 of Hung would obviously be filled with conductive material and electrically connected to S/D regions, because such self align contact is typical in the art, see Liaw (6448140) in fig. 7, Uehara (6573132) in fig. 1.

Regarding claim 17, Hung discloses a semiconductor device including a first region and a second region in fig. 5 comprising: a first gate electrode 6 of a first IGFET in the first region (right side) having a first lower layer electrode 6 formed on a first gate insulating film 4 and a first upper layer electrode 6a formed on the first lower layer electrode 6; a first cap film 8 formed on the first upper layer electrode 6a; a first nitride film 12 on a side surface of the first upper layer electrode 6a; a first oxide film 10 on a side surface of the first lower layer electrode 6; a first etch stop film including a second nitride film 20 formed on the outside of the first nitride film 12 and first oxide film 10, fig. 5; a second gate electrode 6 of a first IGFET in the first region (left side) having a second lower layer electrode 6 formed on a second gate insulating film 4 and a second upper layer electrode 6a formed on the second lower layer electrode 6; a second cap film 8 formed on the second upper layer electrode 6a; a third nitride film 12 on a side surface of the second upper layer electrode 6a; a second oxide film 10 on a side surface of the second lower layer electrode 6; a second etch stop film including a second nitride film 20 formed on the outside of the second nitride film 12 and second oxide film 10, fig. 5; wherein the first IGFET includes a lightly doped drain 16 and the second IGFET does not include a lightly doped drain, fig. 5.

But Hung does not disclose the first nitride film does not cover the side surface of the cap film.

However, Kim discloses a semiconductor device in fig. 2H including a lower gate electrode 22a disposed on a gate-insulating layer 21, and an upper gate electrode 29 disposed on the lower gate electrode 22a, an oxide film 24 on the side surface of the lower electrode 22a and a nitride film 25 on a side surface of the upper gate electrode 29, fig. 2H. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of nitride film 25 teaching of Kim with Hung's device, because it would have prevented transformation of the gate electrode as taught by Kim, see abstract.

9. Claims 21-24, 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0132403 to Hung et al in view of US 6281084 to Akatsu et al.

Regarding claim 21, Hung discloses a semiconductor device in fig. 5, comprising: a first transistor formed in a first region comprising a first upper layer gate electrode 6a formed on and in electrical connection with a corresponding first lower layer gate electrode 6, a first insulating film 10 formed on a majority of a side surface of the first lower layer gate electrode 6, a second insulating film 12 formed on a side surface of the first upper layer gate electrode 6a, the second insulating film 12 having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material, and a first etching stopper film 20 formed on the outside of the first 10 and second insulating films 12, fig. 5, a first etching stop 12 over a majority of an outside

surface of the first insulating film 10 formed on the majority of the side surface of the first lower layer gate electrode 6, wherein the second insulating film 12 has a film thickness of about 5 nm [0020]..

But Hung does not disclose the first etching stop film in contact with a majority of an outside surface of the first insulating film formed on the majority of the side surface of the first lower layer gate electrode.

However, Akatsu discloses a semiconductor device in fig. 2 comprises a lower gate electrode 18 having insulating film 26, and an upper gate electrode 20 having a insulating film 24, fig. 2, the etching stop film 30 in contact with a majority of an outside surface of the insulating film 26 formed on the majority of the side surface of the first lower layer gate electrode 18, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the nitride film 30 teaching of Akatsu with Hung's device, because it would have improved array gap-fill in the high density dynamic random access memories or embedded memories as taught by Akatsu, column 1 line 5-10.

Regarding claim 22-24, Hung discloses the second insulating film 12 comprises SiN [0021], wherein the first insulating film 10 comprises silicon oxide [0020].

With respect to the 'thermal growth' limitation, it does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

With respect to first lower gate electrode has a greater gate length than the first upper layer gate electrode, Hung and Akatsu discloses the general gate length of the lower and upper electrodes. Accordingly, it would have been

obvious to one of ordinary skill in art to use teaching of Hung and Akatsu in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 26, Hung discloses the semiconductor device further including: a second transistor formed in a second region, fig. 5, comprising a second upper layer gate electrode 6a formed on and in electrical connection with a corresponding second lower layer gate electrode 6, a third insulating film 10 formed on a side surface of the second lower layer gate electrode 6 and not on the side surface of the second upper layer gate electrode 6a, a fourth insulating film 12 formed on a side surface of the second upper layer gate electrode 12, the fourth insulating film having a lower thermal growth rate with respect to the second upper layer gate electrode material than the thermal growth rate of the third insulating film with respect to the second lower layer gate electrode material, a second etching stopper film 20 formed on the outside of the third and fourth insulating films, fig. 5, a first transistor source/drain region 16 extending laterally below the second etching stopper film 20, fig. 5, and a second transistor source/drain region 18 overlapping a portion of the first transistor source region that does not extend laterally below the second etching stopper film, fig. 5.

With respect to the 'thermal growth' limitation, it does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 27, Hung discloses the semiconductor device further including a third transistor source/drain region 16 having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film, fig. 5.

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0132403 to Hung and US 6281084 to Akatsu et al and further in view of US 6448140 to Liaw.

Regarding claim 25, Hung does not disclose the semiconductor device wherein the first lower layer gate electrode 6 has a greater length that the first upper layer gate electrode 6a.

However, Liaw discloses the semiconductor device in fig. 7 wherein the first lower layer gate electrode 3, column 3 line 58, has a greater length that the first upper layer gate electrode 4, column 3 line 60. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the gate length teaching of Liaw with Hung's device because it would have created a thicker sidewall layer and resulting in a smooth, non-protruding sidewall layer as taught by Liaw, column 1 lines 60-67.

11. Claims 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0132403 to Hung et al in view of US 6483138 to Habu et al.

Regarding claim 28, Hung discloses a semiconductor device in fig. 5, comprising: a first transistor (left) formed in a first region comprising a first upper layer gate electrode 6a formed on and in electrical connection with a corresponding first lower

layer gate electrode 6, a first insulating film 10 formed on a side surface of the first lower layer gate electrode 6 and not on the side surface of the first upper layer gate electrode 6a, a second insulating film12 formed on a side surface of the first upper layer gate electrode 6a, the second insulating film having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material, a first etch stopper film 20 formed on the outside of the first and second insulating films 10/12 wherein the second insulating film 12 has a thickness of less than 6 nm [0020], a second transistor (right) formed in a second region comprising a second upper layer gate electrode 6a formed on and in electrical connection with a corresponding second lower layer gate electrode 6, a third insulating film 10 formed on a side surface of the second lower layer gate electrode 6 and not on the side surface of the second upper layer gate electrode 6a, a fourth insulating film 12 formed on a side surface of the second upper layer gate electrode 6a, the fourth insulating film 12 having a lower thermal growth rate with respect to the second upper gate layer electrode material than the thermal growth rate of the third insulating film 10 with respect to the second lower layer gate electrode material 6, a second etching stopper film 20 formed on the outside of the third and fourth insulating films 10/12, a first transistor S/D region 16 (right) extending laterally below the second etching stopper film 20, a second transistor S/D 18 (right) region overlapping a portion of the first transistor S/D 16 region that does not extend laterally below the second etching stopper film 20; a third transistor S/D region (left) having a different concentration than either the first and the second transistor S/D

extending laterally below the first etching stopper film 20; the first transistor (left) includes at least a third S/D region.

But, Hung does not disclose the semiconductor device wherein a first contact in electrical connection with the third S/D region, and isolated from the first lower gate electrode 6 by a fist insulating thickness; and a second contact in electrical connection with the first and second S/D region, and isolated from the second lower layer gate electrode 6 by a second insulating thickness that is greater than the first insulating thickness.

However, Habu discloses in fig. 19G the semiconductor device wherein a first contact 13 (left) in electrical connection with the third S/D region 8, and isolated from the first gate electrode 2 by a fist insulating thickness; and a second contact 13 (right) in electrical connection with the first and second S/D region 8/9, and isolated from the second layer gate electrode 2 by a second insulating thickness that is greater than the first insulating thickness. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the contacts teaching of Habu with Hung's device, because it would have created a semiconductor device having a fine transistor capable of reducing resistance of the contact between a wiring layer and a diffusion layer and exhibiting excellent controllability by providing a large are for a contact hole formed in a self-align manner with a gate electrode as taught by Habu in col. 2 lines 58-65.

Response to Arguments

12. Applicant's arguments filed 24 Oct 2005 have been fully considered but they are not persuasive.

- With respect to claim 21-27, the Applicant argues that the thin barrier layer 30 of Akatsu is not a 'etching stopper film'; the film 30 is a barrier layer. This is not persuasive because Akatsu discloses layer 30 is a dielectric material, col. 2 line 64, that may consist of nitride or oxide, col. 3 line 1.Thus, the Examiner submits that the layer 30 of Akatsu would function as a either an etch stopper or barrier material. The recitation of 'etch stopping film' is only a statement of the inherent properties of the material. When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

- With respect to claims 1-3, 5-7, 17-19, and 22-24, the Applicant argues that the combination of Hung and Kim can not be sufficient for a prima facie case of obviousness as it directly contradicts the teaching of Hung et al, and by using layer 25 of Kim will necessarily remove the top nitride layer of Hung's structure. The Examiner respectfully disagrees because both nitride layers 25 of Kim and 12 of Hung provide the same function of preventing oxidation of the gate

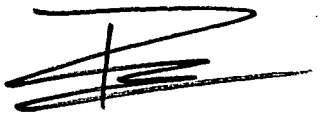
electrode. Thus, using layer 25 of Kim covers ONLY the side wall of upper electrode 6a of Hung and forms the cap layer 8 subsequently would not change the principle of operation of the primary reference or render the reference inoperable for its intended purpose. See MPEP § 2143.01. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference.... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). See also *In re Sneed*, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983). It is not necessary that the inventions of the references be physically combinable to render obvious the invention under review."; and *In re Nievelt*, 482 F.2d 965, 179 USPQ 224, 226 (CCPA 1973). Combining the teachings of references does not involve an ability to combine their specific structures. Thus, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, the prior arts must be considered in entirely, including discloses that teach away from the claims, MPEP § 2143.01-02.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
15 November 2005